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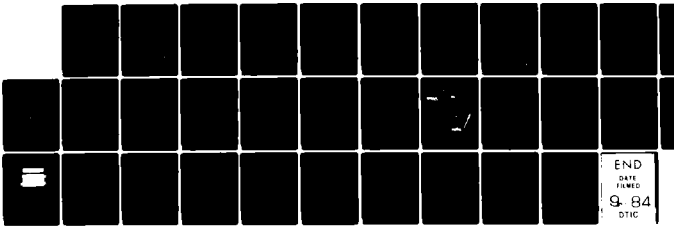

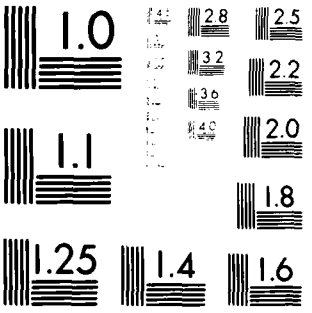

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Manufacturing Methods for Microwave Circuits

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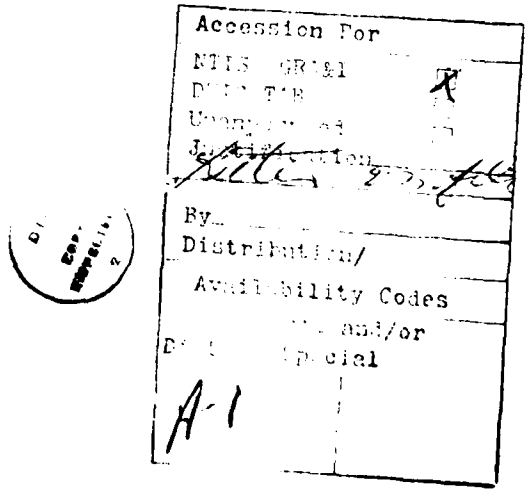

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ABSTRACT

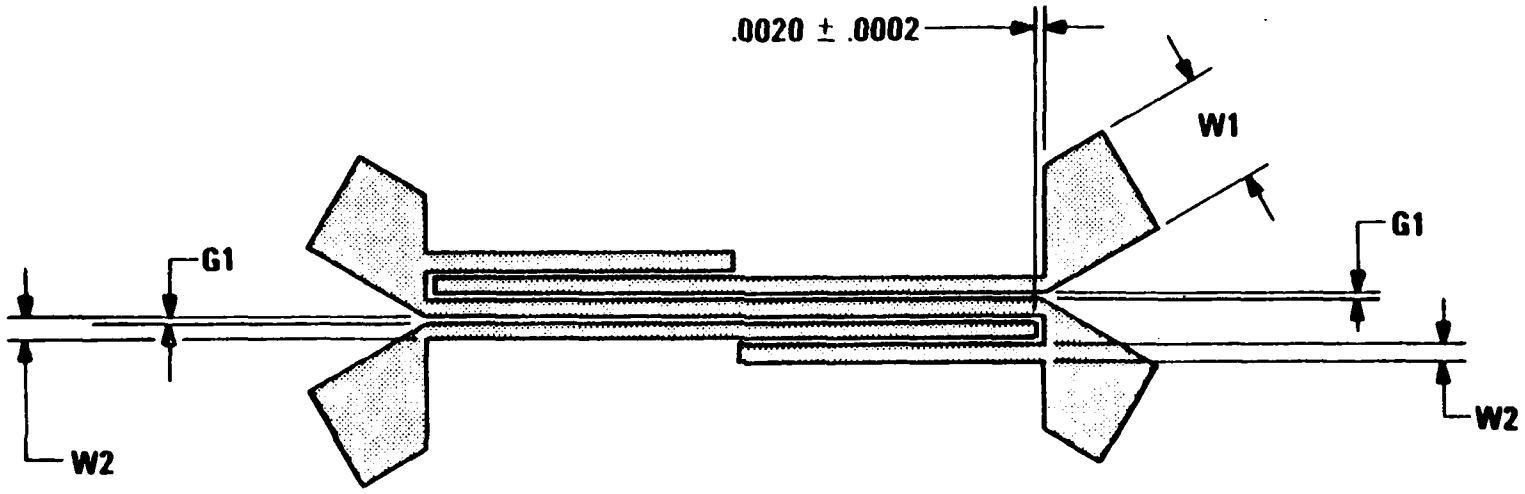
Two processes were investigated to manufacture microwave circuit films on hard dielectric substrates, and each proved superior when compared to the conventional wet chemical etching process. Ion beam milling was developed at the Microwave Division of Sanders Associates, Inc., and its high quality low cost capability instigated replacement of the wet chemical etch process. Up-plating was developed at the Microelectronics Center of the Naval Research Laboratories. Both methods demonstrate substantial improvements in the dimensional film definition achieved in manufacturing microwave circuits.

I. Introduction

Increased complexity of modern military microwave systems compel higher density packaging. Historically this has been reflected in changes in the transmission medium from waveguide to stripline to microstrip. Line width and gap dimensions for a microstrip inter-digitated coupler shown in Figure 1 reflects associated tighter fabrication tolerances. The 2.5 micron (0.0001") tolerance required for this type of component is difficult to achieve using the conventional wet etch process. The uncertain dimensional regulation for the process limits yields making costs prohibitive. This set of conditions instigated support of the ion beam milling and up-plating efforts by the Naval Air Systems Command Manufacturing Technology program office to resolve these problems.

Ion beam milling is a process done under vacuum in which an argon plasma is produced and the argon ions are accelerated and collimated into a beam. The ions bombard the substrate surface and remove particles of the metal surface film by momentum transfer. Using this process we have successfully fabricated circuits films on fused silica (SiO_2), alumina (Al_2O_3), and gallium arsenide (GaAs) with metal film thickness of up to 200 microinches. Ion beam milling is an anisotropic process capable of milling vertical walls and with proper fixturing a specific degree of directionality can be achieved.

TYPICAL CIRCUIT TOLERANCES OF INTERDIGITIZED COUPLER



INSPECTION DATA	
W1	.032 ± .001
W2	.0050 ± .0003
G1	$.0009 \pm \frac{.0001}{.0002}$

SANDERS ASSOCIATES, INC

V-88-0418-005

FIGURE 1

(All dimensions in inches.)

The up-plating process uses polyimide which is plasma etched in a parallel plate etcher with an oxygen plasma to form the channels into which gold is electroplated to produce a circuit film. This process was also used to fabricate circuits on fused silica (SiO_2) and alumina (Al_2O_3).

The program documented ion beam milling and up-plating processes. Seventy-three (73) circuits were produced using ion beam milling; thirty-three (33) circuits were produced using up-plating; and sixty-four (64) circuits were produced using chemical etching. All these circuits were evaluated for dimensional integrity, electrical performance, cost, yield, and comparisons were made to define the best process. Chemical etching was included to provide the basis for comparison.

II. Processing Techniques

A) Ion Beam Milling

The ion beam milling process developed at Sanders Associates, Inc. Microwave Division, employs a specially developed resist process using standard contact photolithography to pattern the circuit image. This resisted pattern has proven to hold up for at least 140 minutes under ion bombardment. The resist process developed for ion beam milling is:

1) Apply liberal amount of outgassed Shipley 1375 positive resist to substrates and spin at 3000 RPM for 20 seconds.

2) Bake at 90°C for 25 minutes to cure resist.

3) Allow substrates to return to ambient in dry nitrogen.

4) Expose pattern for one minute using OAI Hybralign Series 400 contact photolithography system.

5) Develop resist using a spray developer on the following cycles:

   a) 2 minutes Microposit 351 Developer
   b) 4 mintues D.I. water rinse
   c) 2 minutes dry using dry nitrogen

6) Bake substrates for 25 minutes at 125°C to stabilize resist.

7) Allow to return to ambient in dry nitrogen.

8) Final hardness bake for 25 minutes at 150°C.

9) Allow to return to ambient in dry nitrogen.

One of the first problems to be encountered in attempting to ion beam mill microwave circuits is thermal. High milling rates are accomplished by high intense ion bombardment. A great deal of heat is generated in the ion bombardment and early attempts at ion beam milling burned the substrates rather than patterning a circuit. Reducing the ion bombardment activity and angling the substrates in the direction of the ion beam solved this problem. However, increasing the angle also exponentially reduces the milling rate and excessive angling can adversely affect substrate

trace wall angles. After extensive analytical studies, in which the ion impact angle, speed, mass, approximate deflected particle trajectory path and reduced speed were considered, we arrived at a beam control current of 0.680 ma/cm^2 and a work piece angle of ±10°. At these levels, milling a four micron metalization thickness on Al_2O_3 of 635 micron (0.025") thickness produces a tolerable surface temperature of about 100°C.

Another problem encountered in Ion Beam Milling is re-deposition of material on the substrates. To prevent this, an effective pumping envelope must be maintained in close proximity to the work area. The integrity of this Hi-Vac area must be of high quality. Although inert argon ion milling occurs in the 10^{-4} torr range, the Hi-Vac portion of the system must be capable of 10^{-9} torr with all traps (LN_2, H_2O, etc.) full to capacity. The ability of the system to perform properly depends upon the Hi-Vac systems ability to extricate as rapidly as possible the deflected milled atoms. This is accomplished by constantly monitoring the system parameters and regularly shutting the system down and thoroughly cleaning the active Hi-Vac area.

The Ion Beam process to produce microwave circuits on 381 micron (0.015") thick fused silica with a metalization of 1.5-2.3 microns of gold, 2500Å of copper and 200-400 A of chromium is:

1. Place substrates on working fixture and pump down system to 9 X 10^{-6} torr. [Maximum run size 10 5 cm x 5 cm (2" x 2") substrates. Approximate time required, 20 minutes.]

2. Establish argon plasma at 2 X 10^{-4} torr and ion beam current of 0.68ma/cm^2 and mill for 60 minutes angling fixture at ±10° alternating between positive and negative attitude every 10 minutes.

3. Allow system to cool for approximately 20 minutes, then remove substrates.

Through experimentation and analysis, we have found that this process produces high quality microwave circuits with 90% yield and 100% repeatability. We also found that this process reduced inspection; rework and test time; and produced near vertical walls with respect to the substrate surface.

B) Up-Plating

The fused silica substrates used for up-plating were coated with 50 Å of chromium and 1000 Å of gold. After solvent clean and 90°C bake, the first layer of polyimide was spin-coated at 5KRPM (for Hitachi PIQ 13, the corresponding thickness is about 1.5 micrometers), followed by soft bake at 90°C for an hour and then hard bake at 300°C for an hour. A second layer polyimide was subsequently spin-coated and baked under the same conditions. These two layers of polyimide with a total thickness of 3 micrometers formed the first level of resist. The second level was a 1000 A aluminum film evaporated on the polyimide; this aluminum layer would later function as a barrier to the plasma etch of polyimide. To define pattern on aluminum we used Shipley 1370 positive resist and followed standard photolithographic procedures. After etching aluminum, The tri-level structure was ready for polyimide etch. In this work, an E.T. Equipment 317 parallel plate etcher was used. The polyimide was etched in oxygen plasma under pressure of 0.2 Torr and R.F. current of 1.0 Amp

for 30 minutes. During this etching step, the aluminum layer acts as a barrier to the oxygen plasma. However, the parallel plate etcher provides anisotropic etching which removes the exposed polyimide down until stopped by the gold, resulting in an almost vertical wall profile. Figure 2a shows the tri-level structure developed after polyimide etch. Prior to gold plating, the aluminum barrier was etched off. To reduce both plating time and gold consumption, the backside of the substrate was coated with positive resist and baked. The Lea-Ronal Aural 292M process was used for up-plating of gold pattern. The desired thickness can be obtained by careful control of plating time and current. The vertical wall of the gold pattern is the replica of the plasma etched polyimide as shown in Figure 2b. The final circuit board was obtained by etching in oxygen plasma to clear all polyimide, followed by stripping the thin background gold and backside resist.

C) Chemical Etching Process

A control lot using identical circuit masks was produced using wet chemical etching. This lot was tested with those produced by ion beam milling and by up-plating to provide a basis of evaluation. The chemical etching process used was:

A. Clean substrates and apply and pattern photoresist as detailed for the ion beam milling process. We use the same photoresist process for both chemical etching and ion beam milling and can process in lots of 10 through this stage.

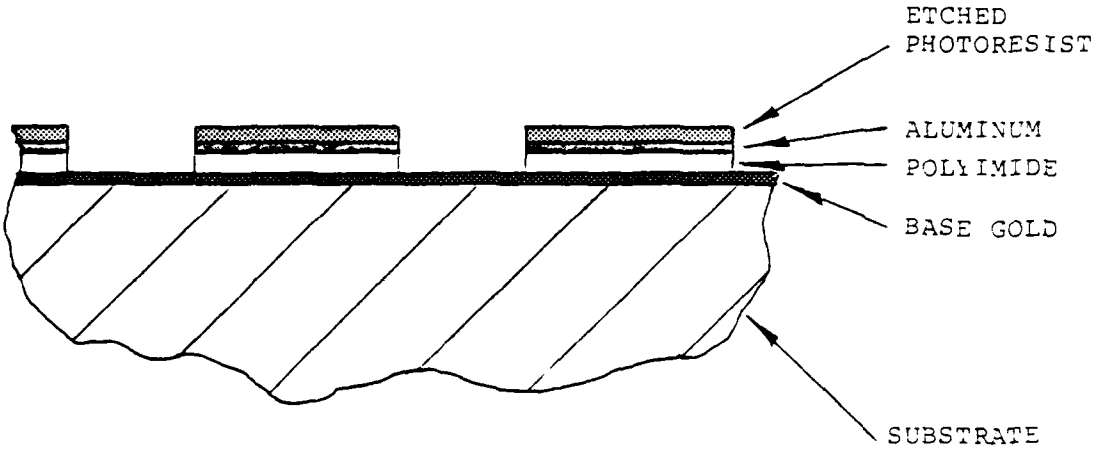


FIGURE 2a: TRI-LEVEL STRUCTURE DEVELOPED AFTER PLASMA ETCHING OF POLYIMIDE.

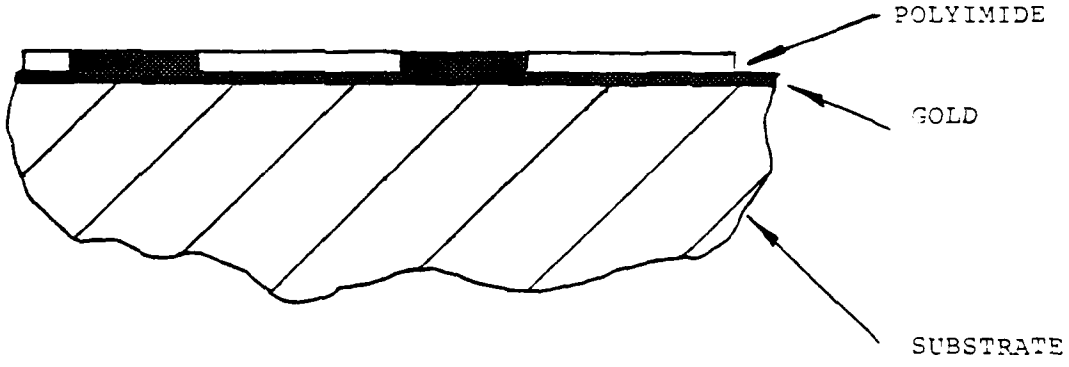


FIGURE 2b: THE PLATED GOLD IS SEEN AS THE REPLICA OF THE PLASMA ETCHED POLYIMIDE.

B. Tape the backside of substrate to prevent etching of ground plane.

C. Etch gold using C35 etchant by Film Microelectronic with an etch rate of 650Å/sec at 75°C.

1. Dip into etchant bath and agitate until gold appears etched on some portion of substrate.

2. Rinse in D.I. water.

3. Inspect and touch up etched areas with krylon paint to prevent further etching.

4. Repeat steps 1 to 3 until gold pattern is completely etched.

5. Wash with acetone.

6. Inspect and scrape off any remaining gold flakes.
NOTE: This process also etches the thin copper layer we are using.

D. Etch chromium using Transene TFD etchant with etch rate of 40A/sec.

1. Dip into etchant bath and agitate until chrome appears etched.
2. Rinse in D.I. water.
3. Inspect and repeat steps 2 and 3 as needed.

E. Remove backing from substrate.

F. Inspect and clean up substrates.

This etching process takes approximately 1½ hours per substrate processed one at a time starting with a patterned resist.

D) Electrical Test Procedure

The circuits produced to evaluate these processes were frequency discriminator networks (FDN) used in Digital Instantaneous Frequency Measurement (DIFM) receivers. The theory of operation for DIFMs is well established in the literature (refer to P.W. East, IEEE Proc. Vol. 129, Pt. F, No. 3, June 1982). The FDN resolves RF frequency by measuring the phase length across a fixed length of transmission line. This performance was evaluated for the microstrip FDN circuits produced during the program. To resolve frequency the circuit divides the signal and one component is delayed before the pair is applied to inputs of a phase resolving section. The resolver consists of four (4) interdigitated couplers and a Schiffman 90° phase element. This combination is arranged to provide 4 quadrature phased outputs that vary as a function of frequency. These outputs are detected employing interdigitated couplers to mask reflections. The amplitudes of the detected outputs vary as a function of frequency and are processed to identify frequency. For the FDN to function properly it is essential that component phase errors be minimal. To evaluate circuit quality we measured the phase characteristics and applied linear regression analysis to electrically evaluate performance.

The actual testing consisted of measuring the voltage amplitude of the detector outputs over a frequency range. Using these values the phase angle is then calculated for each frequency and this data is plotted to obtain a continuous phase plot. A linear regression analysis of phase vs. frequency is performed to obtain the line that represents the best straight line fit to the actual data. The measured data is then compared to this best straight line fit to generate a plot of phase deviation at each test frequency.

These plots provide a quantitative evaluation of the FDN electrical performance which establishes a basis for verifying electrical effects of circuit film dimensional deviations. This data base was implemented using a computer controlled Hewlett Packard 3437A system voltmeter currently employed in DIFM manufacturing.

III. Results

To evaluate these three processes, seventy-three (73) circuits were fabricated using ion beam milling, thirty-three (33) circuits using up-plating, and sixty-four (64) by chemical etching. These circuits were evaluated 100% for line width and gap dimensions. A few circuits were examined using a scanning electron microscope (SEM). All circuits were assembled into housings to provide connections for performing electrical testing.

All the circuits produced in this program were 100% inspected for critical dimensions. These circuits were produced on 5 cm x 5 cm (2" x 2") fused silica (SiO_2) substrates and measure 1.8 cm x 3.5 cm (0.704" x 1.385") after cutting. Each of these circuits contain 8 of the interdigital structures shown in Figure 1. The gap, G1, is the most critical dimension and was measured at several points on at least two couplers on each circuit using a Vickers microscope equipped with a split image wire strain measurement system. The average gap dimension was then obtained by taking the mean of these measurements for each circuit. This inspection was done in accordance with approved quality assurance procedures. Ion beam milling produced an average G1 of 21.6 microns (0.00085"), up-plating 17.3 microns (0.00068"), and chemical etching 25.2 microns (0.00099") from masks on which G1 measures 20.3 microns (0.00080").

Masks having a correction factor of approximately 2.5 micron (100 microinches) added to each line for up-plating would produce circuits which are all within tolerance. This factor was not added to the mask set we used because we wished to use identical masks to evaluate each process. The data shows chemical etching and up-plating produce opposite effects on the circuit line and gap dimensions. The masks were produced with 20.3 micron (0.00080") gaps to allow for chemical etching to produce circuits within tolerances. This resulted in slightly under sized gaps being produced by up-plating.

Figure 3 is a frequency distribution histogram of the data collected for each process, and figure 4 is the gaussian distribution of this data. The gaussian distributions show that ion beam milling has a standard deviation of 0.36 microns (±14.26 microinches), while up-plating produced a standard deviation of 0.61 microns (±24.16 microinches), and both had excellent repeatability. Chemical etching had a standard deviation of 1.3 microns (±52.29 microinches) with poor repeatability.

SEM micrographs were taken from circuits fabricated by each process. The line edge profiles obtained are shown in Figure 5a for chemical etching, Figure 5b for ion beam milling, and Figure 5c for up-plating. It is clear that the wet chemically etched sample has poor edge acuity and an undercut gold pattern. For ion beam milling and up-plating the gold pattern definition is far superior. The ion beam milled edge profile shows a rounding of the top edge of the wall and some overmilling into the substrate material. A further polishing of the substrate surface by ion beam milling can also be seen. For the up-plated sample the wall is seen to be the replica for the plasma etched polyimide with nearly vertical walls and a sharper top edge. Some artifacts of the sample preparation process for SEM can also be seen in each micrograph.

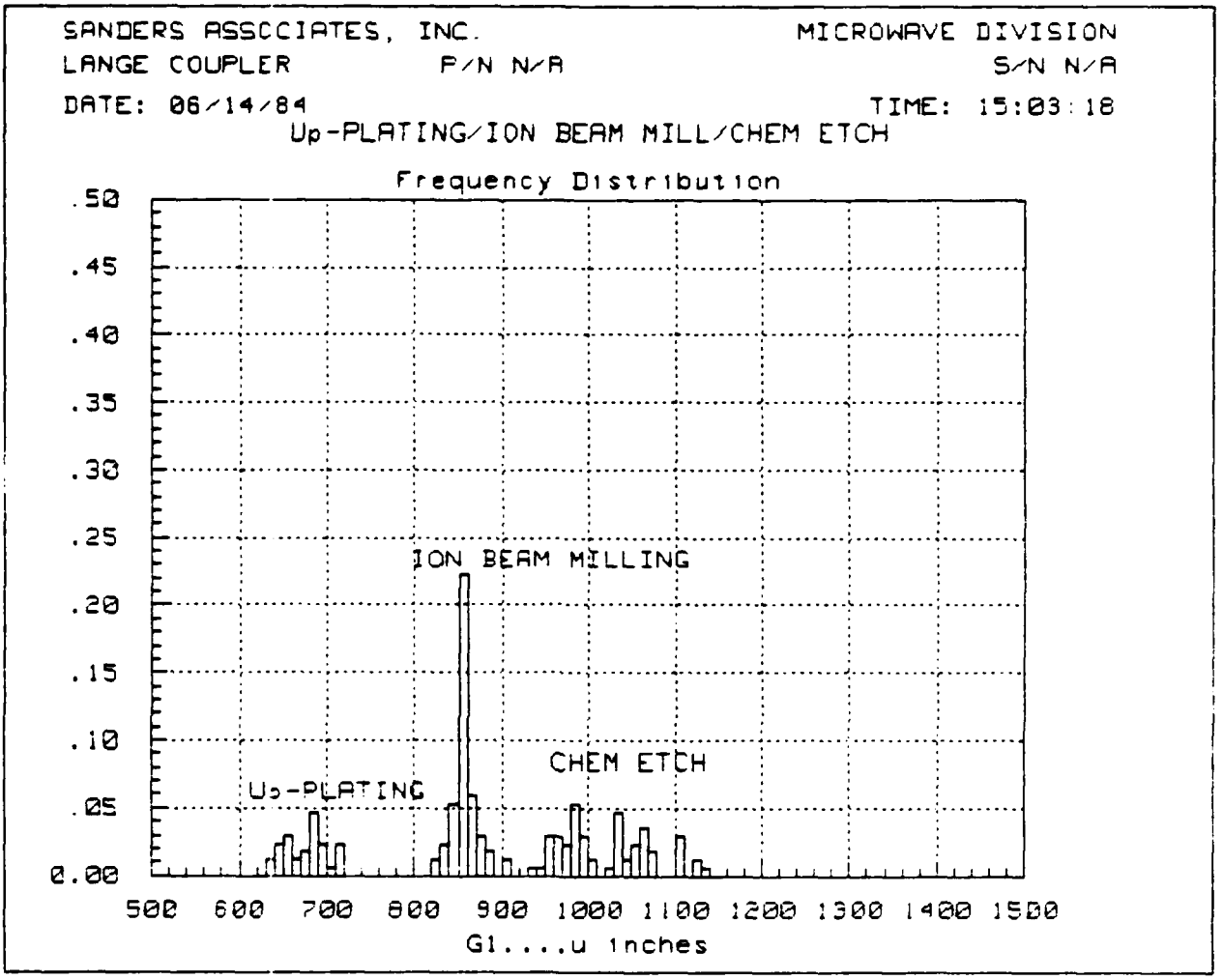


FIGURE 3: FREQUENCY DISTRIBUTION HISTOGRAM OF GAP G1 DIMENSIONS FOR UP-PLATING, ION BEAM MILLING, AND CHEMICAL ETCHING. (NORMALLIZED OCCURANCES vs. MEASUREMENTS IN MICROINCHES)

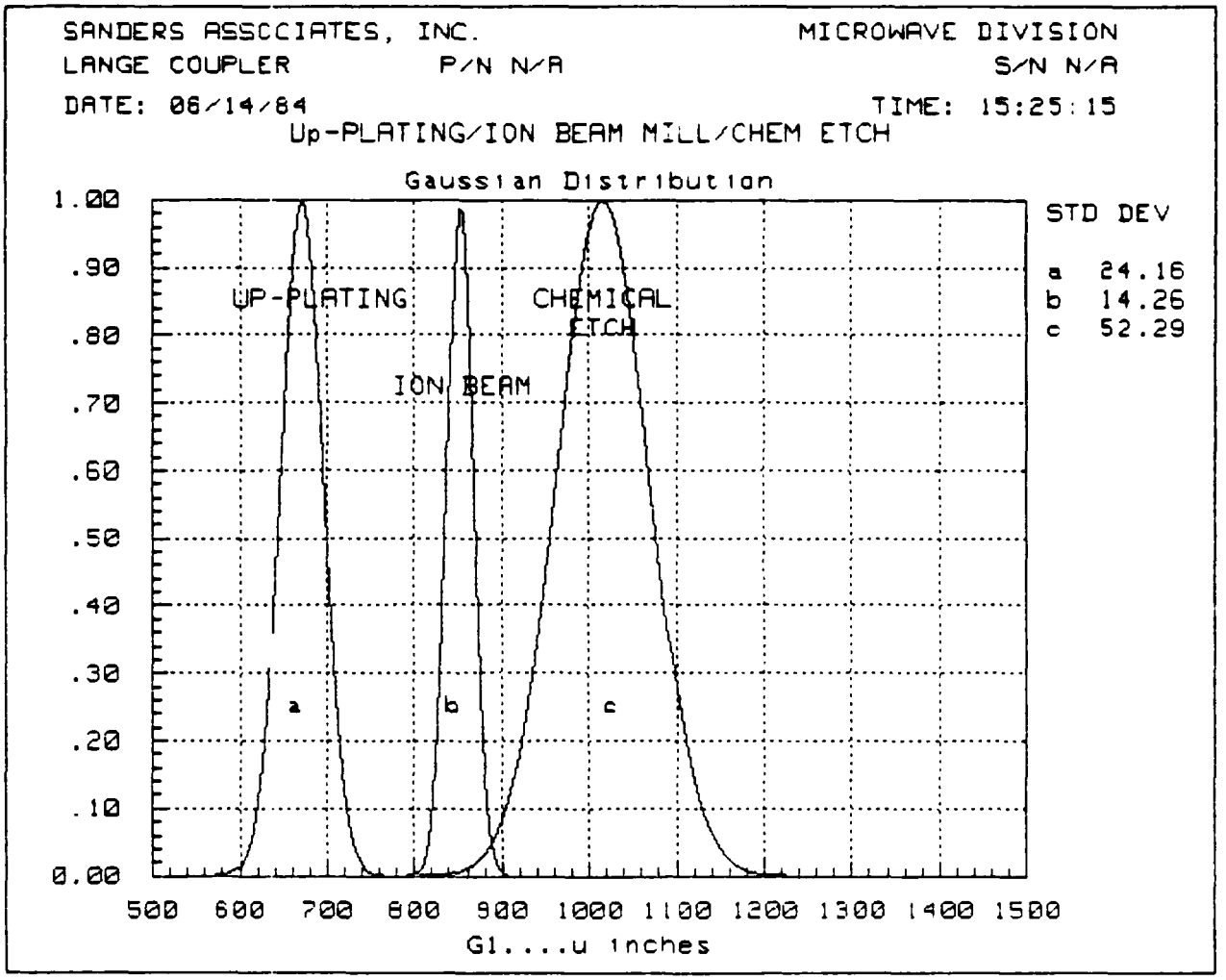
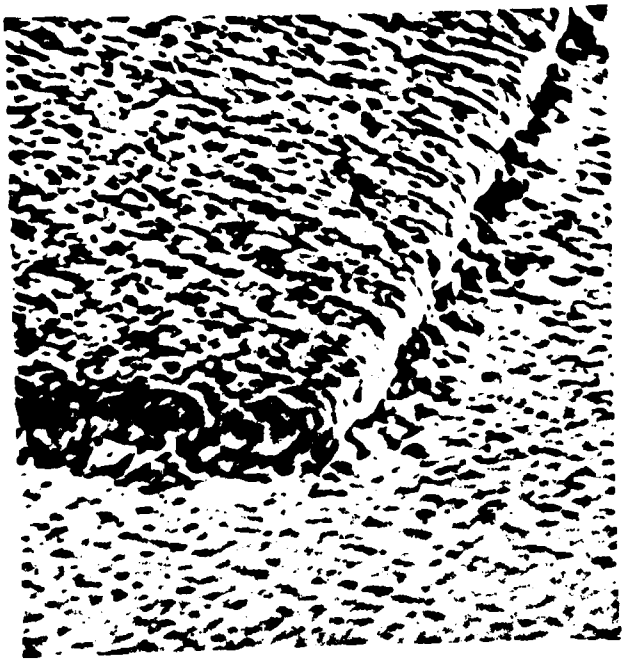
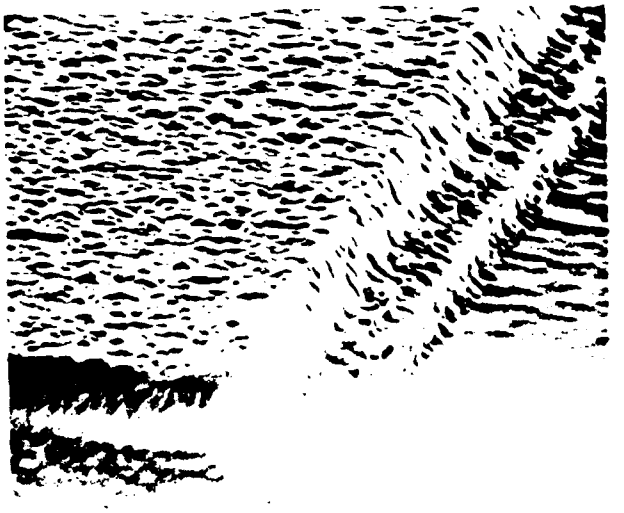


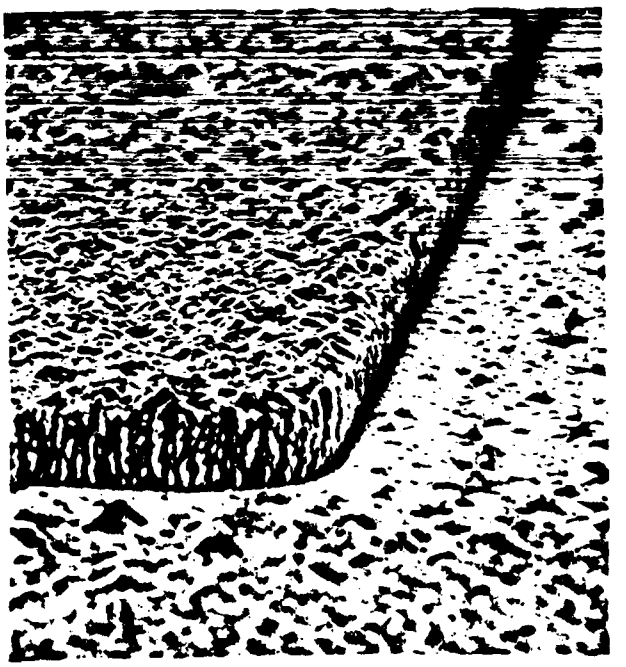
FIGURE 4: GAUSSIAN DISTRIBUTION OF GAP G1 DIMENSIONS FOR UP-PLATING, ION BEAM MILLING, AND CHEMICAL ETCHING.



(a) WET CHEMICAL ETCHING



(b) ION BEAM MILLING



(c) UP-PLATING

FIGURE 5: SEM MICROGRAPHS OF GOLD CIRCUIT LINES PRODUCED BY (a) WET CHEMICAL ETCHING, (b) ION BEAM MILLING, (c) UP-PLATING.

Electrical testing was performed on the assembled circuits as outlined earlier in this report. All processes produced circuits with good electrical results if the tolerances required in figure 1 were met. Also the up-plated circuits with slightly undersized gaps produced good results as determined from computer analysis of the circuit model. Five (5) versions of FDNs with X4 delay relationships were produced by each process and each of these networks had a given phase error tolerance derived from the system application.

Figure 6 shows the results for an ion beam milled least significant resolver. Figure 7 shows the results for a chemically etched resolver of the same type. For this resolver network we would like to see as little phase error as possible but ±5° must be maintained. The ion beam milled circuit in figure 6 with a phase error of ±1.5° shows excellent data and the chemical etched circuit in figure 7 with a phase error of ±5° shows acceptable data. Figures 8 and 9 show the test results for two up-plated circuits of the two next most significant resolvers. For these networks we need to maintain phase errors of ±8°. The data in figure 8 shows ±8° while the data in figure 9 shows ±6.5° indicating that these are both good parts. In figure 10 are the test results for an ion beam milled most significant resolver which requires a phase error of ±12°. As can be seen this network showed ±9° phase error limits. The best conclusion that can be reached from the electrical test results is that all processes yield electrically good parts if the fabrication tolerances are met. However, the trends showed better electrical results for the ion beam milled and up-plated circuits. A photograph of one of the units produced is shown in figure 11.

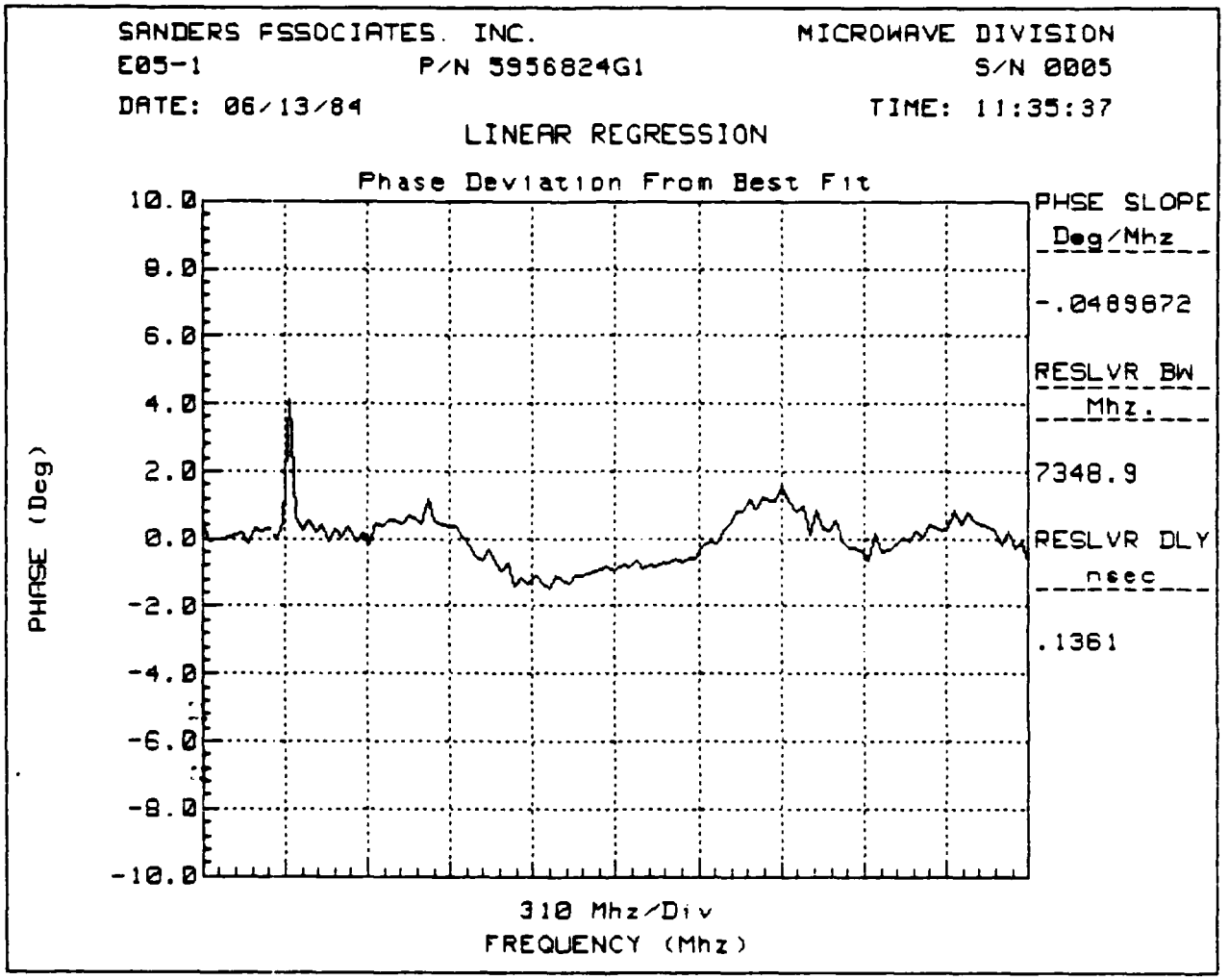


FIGURE 6: ION BEAM MILLED LEAST SIGNIFICANT RESOLVER ELECTRICAL TEST RESULTS.

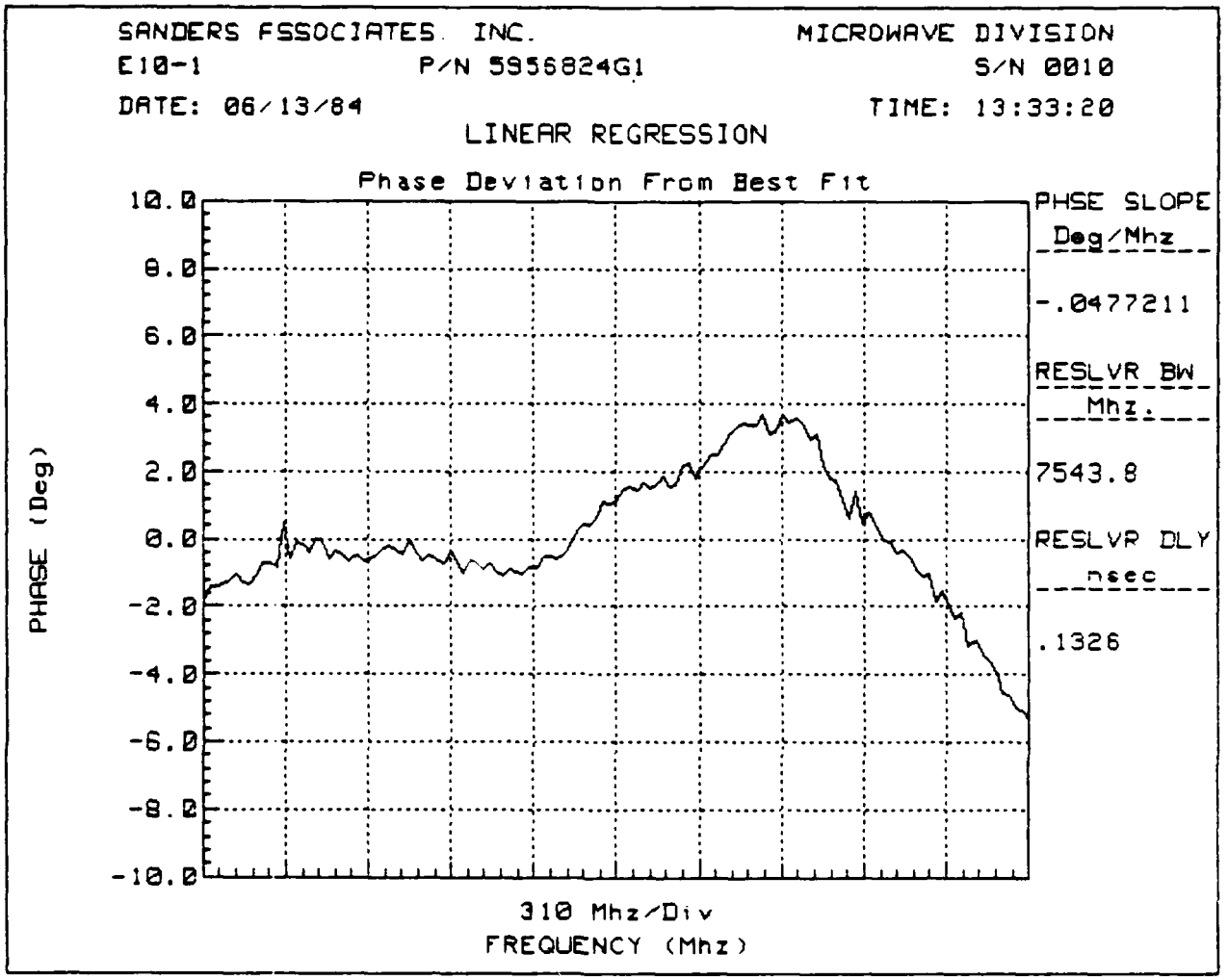


FIGURE 7: CHEMICALLY ETCHED LEAST SIGNIFICANT RESOLVER ELECTRICAL TEST RESULTS.

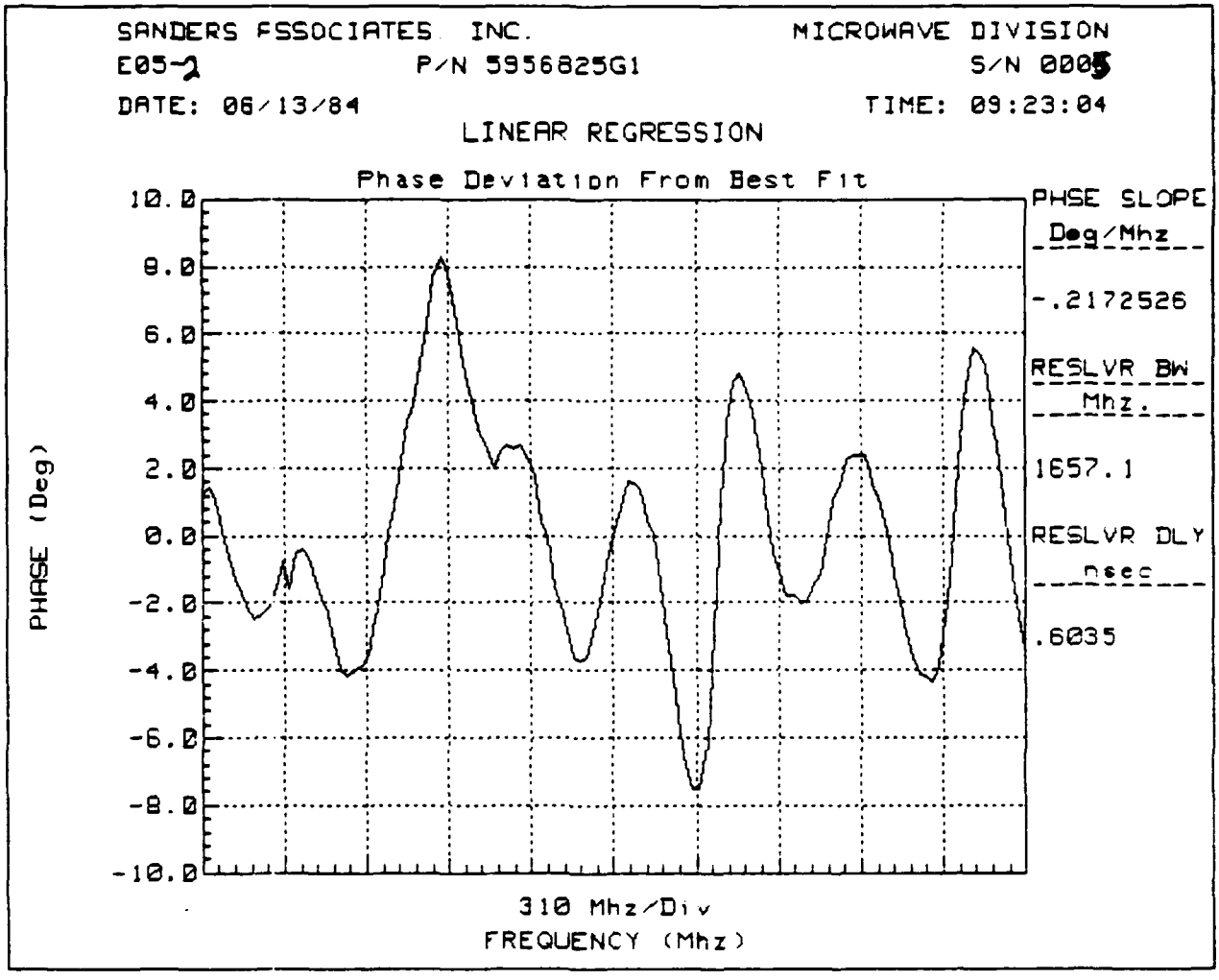


FIGURE 8: UP-PLATING ELECTRICAL TEST RESULTS.

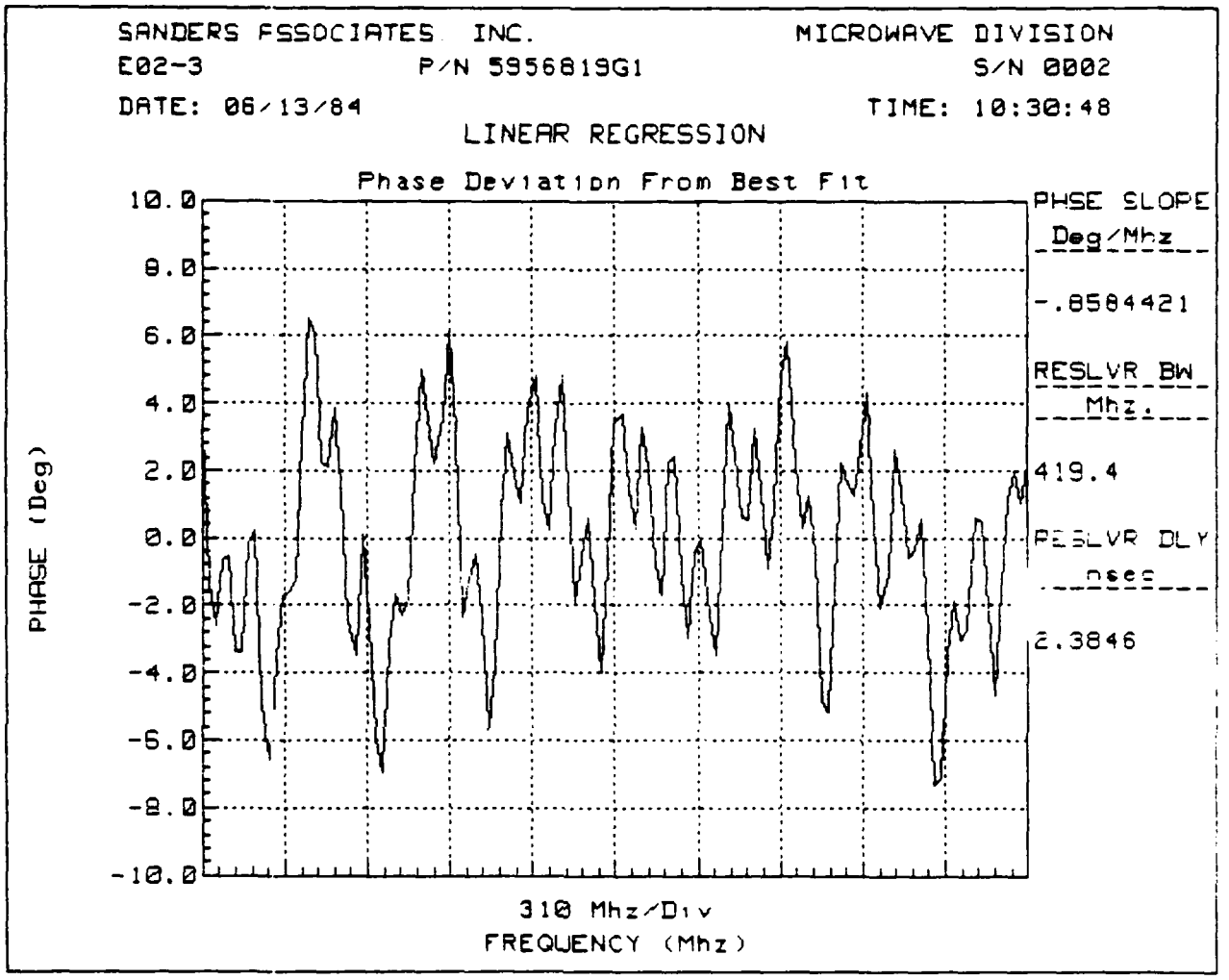


FIGURE 9: UP-PLATING ELECTRICAL TEST RESULTS.

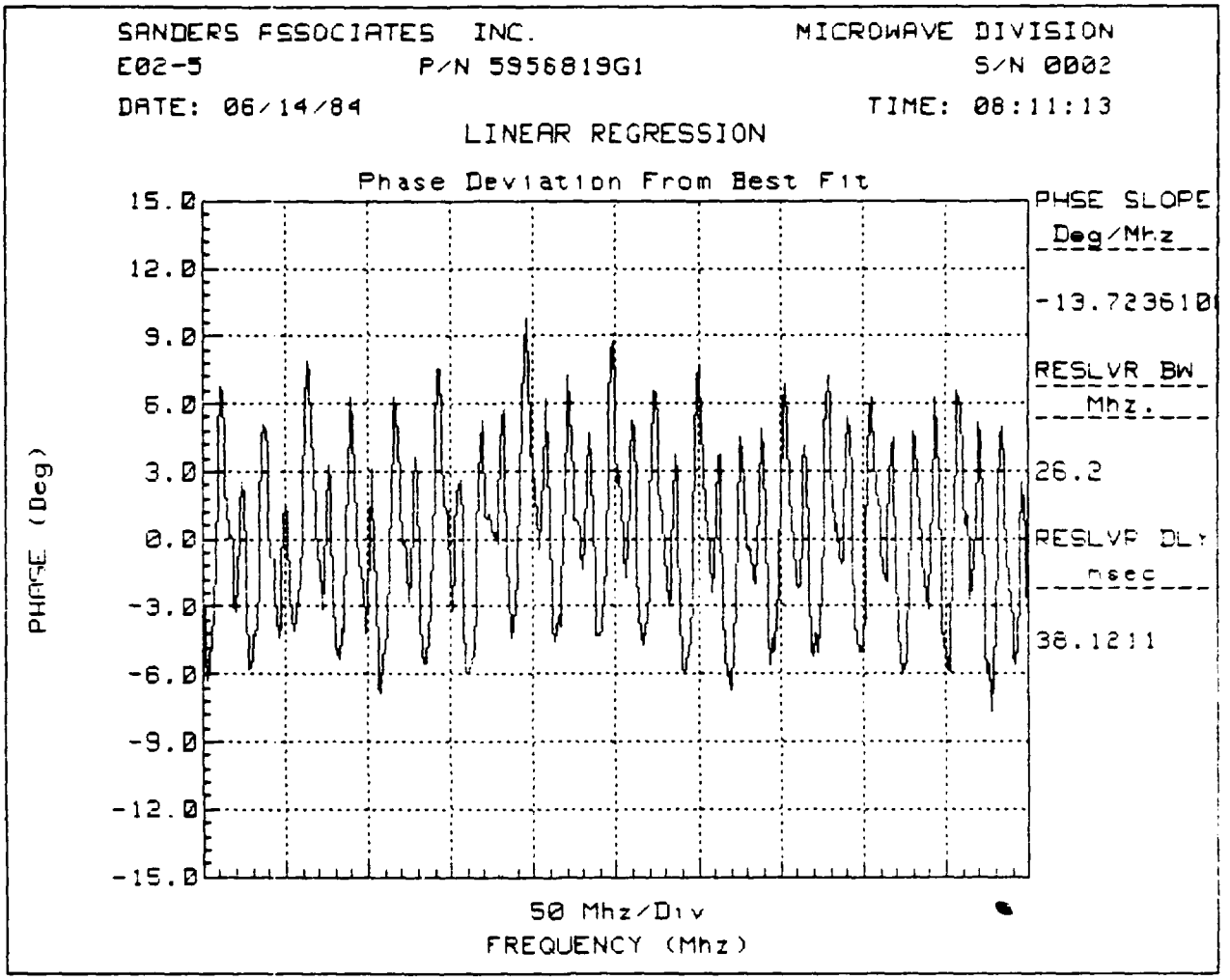


FIGURE 10: ION BEAM MILLED MOST SIGNIFICANT RESOLVER ELECTRICAL TEST RESULTS.

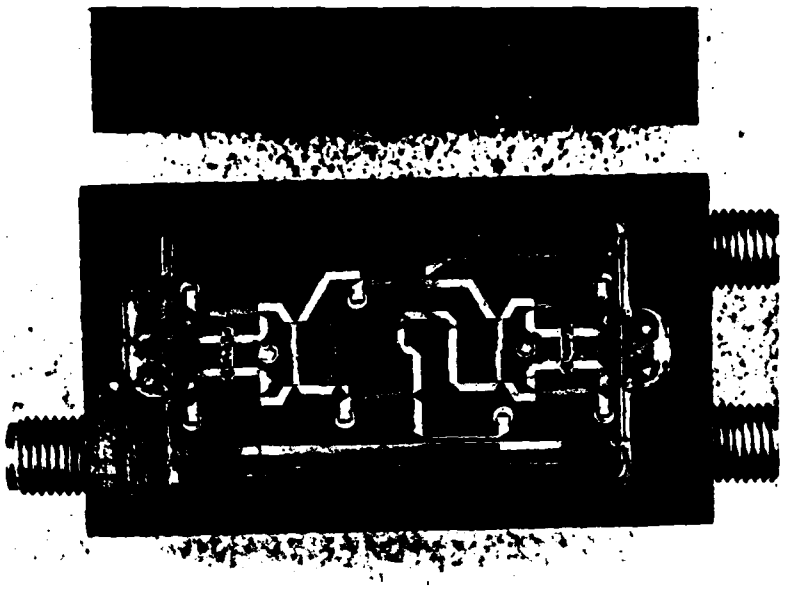


FIGURE 11. PHOTOGRAPH OF PHASE RESOLVER NETWORKS

To obtain labor cost data two independent methods were used. The primary method was to log the start and end time of each process step and labor time expended on that step. The second method was to track the total manhours charged to the work orders used to produce these circuits. The results obtained by both methods were in very close agreement. The key variables derived from this analysis were yield and manhours required to produce a good circuit. These variables are shown for each process in Figure 12. Ion beam milling proved to have the highest yields and lowest cost with chemical etching yields being the lowest and cost the highest. Up-plating fell between ion beam milling and chemical etch in both categories.

	Ion Beam Milling	Up-Plating	Wet Chemical Etching
Good circuits produced (G)	65	26	20
Rejected circuits (R)	8	7	44
Yield $\left(\frac{G}{G+R} \times 100\%\right)$	89%	79%	31%
Man-hour per good circuit	45 min.	145 min.	306 min.

FIGURE 12

Summary of yield and man-hour cost of Ion Beam Milling, Up-plating, and Wet Chemical Etching.

IV. Summary and Conclusions

Increased complexity of modern microwave circuits compels the microwave industry to search for an alternate to wet chemical etching. During this program an ion beam milling and an up-plating process were developed. These processes are illustrated in the process flow diagrams. Figure 13 summarizes the ion beam milling process and Figure 14 the up-plating process. The program established both ion beam milling and up-plating are far superior to chemical etching as can be seen in Figure 15 which compares the processes. Ion beam milling is the superior approach for moderate to high volume production facilities where the larger capital investment (approximately $200,000) can be justified. Up-plating with its lower capital investment (approximately $100,000) appears to be suited for low volume production facilities. Chemical etching with its poor line quality, repeatability, and yields proved to be an almost unworkable process for producing critically dimensioned microwave circuits.

A) Implementation

The ion beam milling process described in this report has been fully implemented in manufacturing at the Microwave Division of Sanders Associates, Inc. Ion beam milling is the primary method used to pattern microwave integrated circuits on hard dielectric substrates such as alumina (Al_2O_3) and fused silica (SiO_2). The switch over from wet chemical etching to ion beam milling was a straight forward effort once the ion beam milling process was established. Modified photolithography techniques used for wet chemical etching were applied to pattern for

FIGURE 13

PROCESS FLOW DIAGRAM FOR ION BEAM MILLING

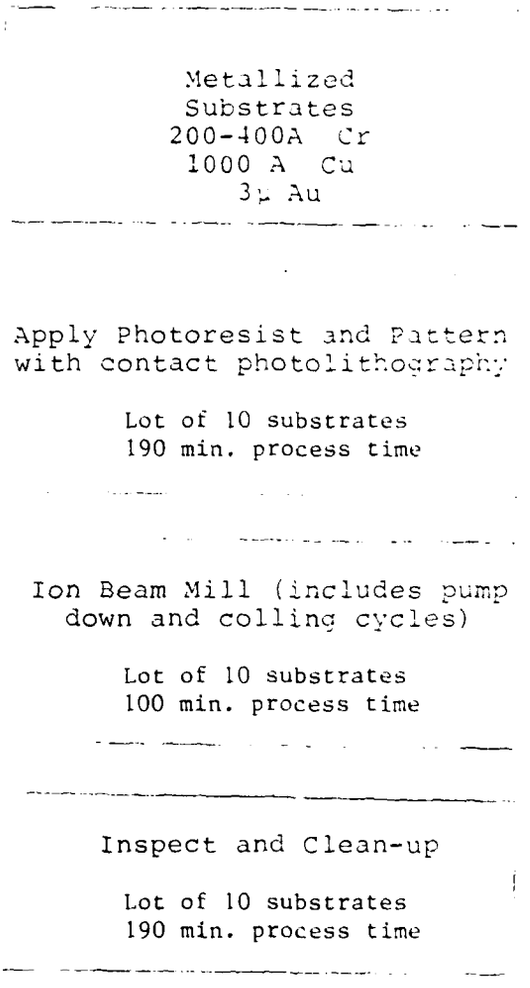
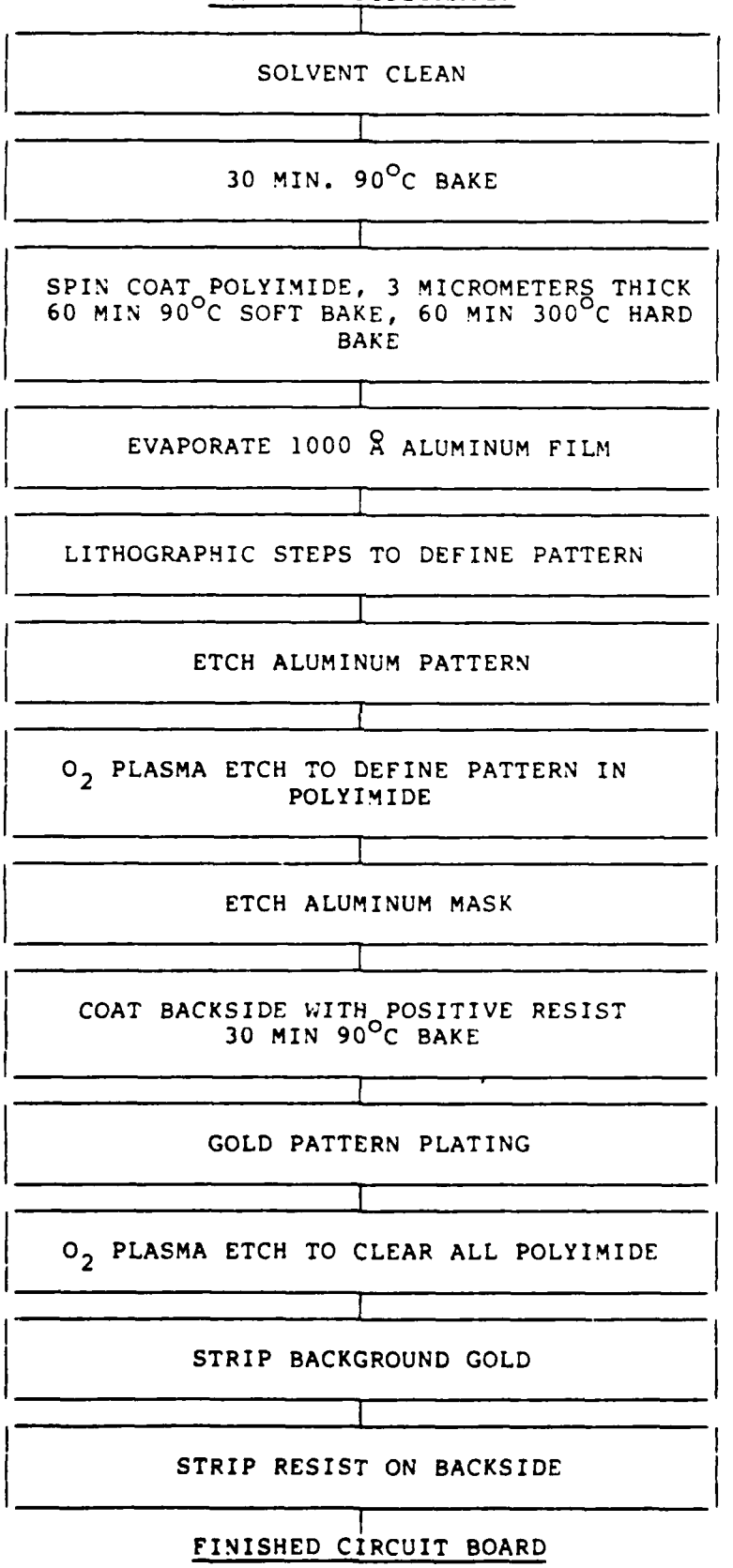


FIGURE 14

PROCESS FLOW DIAGRAM FOR UP-PLATING



	Ion Beam Milling	Up-Plating	Chemical Etching
Processing Cost	Low	Moderate	High
Yield	High	High	Low
Line Quality	Good	Good	Poor
Repeatability	Excellent	Excellent	Poor
Capital Investment*	$200,000	$100,000	$00

FIGURE 15: COMPARISON OF ION BEAM MILLING, UP-PLATING, AND CHEMICAL ETCHING.

* Note: Assumes UV contact photolithography is in place and same equipment used for each process.

ion beam milling. The only tooling changes involved a simplification involving the removal of the photomask etch factors needed to compensate undercutting experienced. The ion beam milling process has provided a lower cost, higher throughput capability.

B) Benefits

Sanders Associates has realized many benefits in instituting ion beam milling as a replacement for wet chemical etching as a production process. Circuit designs that could not be economically realized in production before are now routine because of the order of magnitude improvement in circuit definition available from ion beam milling. The high yields and repeatability of ion beam milling make manufacturing material flow easier and more precise to manage. Finally, the cost savings have been significant. The 261 minutes of labor time saved per good circuit produced reported earlier in this report is being realized in production. We project a cost savings on such electronic countermeasure systems as the AN/ALQ-126B, AN/ALQ-135, and the AN/ALQ-137/94 Update to total more than $7 million. This reflects savings potential at Sanders Associates, Inc. and should be significantly amplified when applied to the broader defense electronics manufacturing community.

I have read and approved the final report for Contract Number N00014-82-C-2302, Manufacturing Methods for Microwave Circuits.

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Dr. Steve S. Y. Mak
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Microwave Division
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Dr. Martin Peckerar
Naval Research Laboratory

GLOSSARY

A	angstrom or 10^{-10} meter
C	centigrade
DIFM	digital instantaneous frequency measurement
D.I.	deionized
FDN	frequency discriminator networks
SEM	scanning electron microscope


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LME